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APPLICATION FOR UNITED STATES LETTERS PATENT

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For: IMAGE ENCODER AND METHOD OF ENCODING TO WEIGHT OF PORTIONS
Docket No.: 01N026-US

IMAGE ENCODER AND METHOD OF ENCODING IMAGES ACCORDING TO WEIGHT OF PORTIONS OF IMAGE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an image encoding technique for compressing images, and, more particularly, to an image encoding technique which is suitable for a TV conference system or TV telephone system and which enables to transmit the important image portion of a whole image, such as a person's image, etc. by compressing according to weight of each portion of the whole image.

Description of the Related Art

Like TV conference systems or TV telephone systems, in the case where motion pictures or static images are compressed to lower an amount of data to be transmitted.

FIG. 7 is a circuitry block diagram showing an example of an image encoder.

In FIG. 7, a frame divide circuit 101 divides an input image of one frame into an (N×M) number of blocks, writes the divided input image into a frame memory 102, and also inputs the input image to a motion prediction circuit 103. The frame memory 102 sets the written image to be delayed by one frame and inputs the delayed image to the motion prediction circuit 103. The motion prediction circuit 103 compares each block (target block) included in the frame input from the frame divide circuit 101 with a block of a previously-input frame input from the frame memory 102, which is in the same position as the position of the target block and also with its neighboring blocks of the block of the previously-input frame input from the frame memory 102, and selects a block from the compared blocks of the previously-input frame input from the frame memory 102. Then, the motion prediction circuit 103 detects a difference between the positions of the target block and the selected block to decide a movement of the target block, and sets the movement as a motion vector. An interframe prediction circuit 104 detects the position of the selected block of the previously-input frame which corresponds to the

target block based on the motion vector value obtained from the motion prediction circuit 103, and calculates the differential data which represents the difference between the target block and the selected block of the previously-input frame. Then, the interframe prediction circuit 104 creates image data based on the calculated differential data in combination with the motion vector.

An orthogonal transformation circuit 105 performs DCT (Discrete Cosine Transformation) for the differential data by each block. A quantization circuit 106 quantizes data received from the orthogonal transformation circuit 105 by a step width informed from a quantization step width calculation circuit 110. An encoding circuit 107 encodes the quantized data and the motion vector value into a variable-length code, and stores the quantized data in a transmission buffer circuit 108. After this, the stored data is transmitted to a transmission path at a constant rate in accordance with a transfer rate. A buffer-storage amount detection circuit 109 detects an amount of data stored in the transmission buffer circuit 108, and informs the quantization step width calculation circuit 110 about the detected amount of data stored therein. The quantization step width calculation circuit 110 calculates a quantization step width in accordance with the storage amount, and informs the quantization circuit 106 of the calculated quantization step width.

Unexamined Japanese Patent Application KOKAI Publication No. H6-169452 discloses an image compression technique which is an improved form of the above-described image compression technique. This prior art technique disclosed in the publication will now be explained with reference to FIGS. 8 and 9.

FIG. 8 is a circuitry block diagram showing an image encoder employing the image compression technique disclosed in Unexamined Japanese Patent Application KOKAI Publication No. H6-169452. In FIG. 8, a frame divide circuit 201, a frame memory 202, an interframe prediction circuit 204, an orthogonal transformation circuit 205, a quantization circuit 206, an encoding circuit 207, a transmission buffer circuit 208 and a